APPENDIX B

Figure 20 is a schematic diagram illustrating an example of an input stage of an offsetable differential receiver in accordance with an embodiment of the invention. A differential input signal is coupled to an input 2001 at a gate of a first input transistor 2003 and to an input 2002 at a gate of a second input transistor 2004. A source of the first input transistor 2003 and a source of the second input transistor 2004 are coupled to a first terminal 2011~~9~~ of current source 2012~~0~~. A second terminal 20~~2~~13 of current source 2012~~0~~ is coupled to ground.